EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window H

- Drafts
- Pending
- Active
  - L7: (3477946) power or voltage
  - L8: (457422) clock
  - L9: (2) 6 same 7 same 8
  - L11: (33) 6 same (7 or 8)
  - L6: (127) memory adj module adj controller
  - L12: (1834) module adj controller
  - L13: (2) ("6587912").PN.
  - L14: (2) ("6587912").PN.
  - L15: (9) ("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6...
  - L16: (0) 6 and 15
  - L17: (0) 12 and 15
  - L18: (5799) memory adj module
  - L19: (369) 7 with 18
  - L20: (24) 7 with 8 with 18
- Failed
- Saved
- Favorites
- Tagged (4)
- UDC
- Queue
- Trash

	U		Document ID	Issue Date	Inventor	Current OR	Pages	
1	☐	☑	US 5566318 A	19961015	Joseph, James D.	711/118	14	C v
2	☐	☑	US 5289377 A	19940222	Yokote, Timothy A. et al.	701/35	8	F a
3	☐	☑	US 4451880 A	19840529	Johnson, Robert B. et al.	711/157	43	M c
4	☐	☑	JP 08273355 A	19961018			5	P c

BRS form | IS&R form | Hits | Details | HTML

Ready NUM

DERWENT-ACC-NO: 1997-004208

DERWENT-WEEK: 200167

TITLE: **Power** down memory control unit for DRAM - prohibits supply of control timing signal to failed **memory module,** based on which supply of **clock** signal is also deterred and forced refresh operation is performed by various **memory modules**

PATENT-ASSIGNEE: NEC KOFU LTD[NIDE]

PRIORITY-DATA: 1995JP-0071940 (March 29, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 08273355 A	October 18, 1996	N/A	005	G11C 011/403
JP 3219964 B2	October 15, 2001	N/A	003	G11C 011/41

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 08273355A	N/A	1995JP-0071940	March 29, 1995
JP 3219964B2	N/A	1995JP-0071940	March 29, 1995
JP 3219964B2	Previous Publ.	JP 8273355	N/A

INT-CL (IPC): G06F012/00, G11C011/403 , G11C011/41

ABSTRACTED-PUB-NO: JP 08273355A

BASIC-ABSTRACT:

The control unit comprises a control timing generator circuit (1) and a gate control circuit (2). The timing generator supplies timing control signals (1A-1D) to a number of memory modules (3-6) which perform read-out/write-in operation, in synchronization with a clock signal (11), supplied through gate circuits, typically AND gates (7-10). The gate control circuit provides gating signals (2A-2D) to each of the gate circuits.

When the memory module fails, supply of timing control signal to that module is deterred. A scram of clock signal occurs by which the various other memory modules recognize the operational failure of their counterpart and suspend their operation. A forced refresh operation is then performed for a constant cycle time.

ADVANTAGE - Reduces power consumption. Preserves data of memory module that exhibits operational failure, in tact. Removes overhead during recovery of failed memory module.

CHOSEN-DRAWING: Dwg.1/5

TITLE-TERMS: **POWER** DOWN MEMORY CONTROL UNIT DRAM PROHIBIT SUPPLY CONTROL TIME
SIGNAL FAIL **MEMORY MODULE** BASED SUPPLY **CLOCK** SIGNAL DETER FORCE REFRESH OPERATE PERFORMANCE VARIOUS **MEMORY MODULE**

DERWENT-CLASS: T01 U13 U14

EPI-CODES: T01-H01B; T01-L01; U13-C04B1A; U14-A03B4; U14-A07C;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1997-003774

EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window

- Drafts
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- Active
  - L7: (3477946) power or voltage
  - L8: (457422) clock
  - L9: (2) 6 same 7 same 8
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  - L6: (127) memory adj module adj controller
  - L12: (1834) module adj controller
  - L13: (2) ("6587912").PN.
  - L14: (2) ("6587912").PN.
  - L15: (9) ("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6...
  - L16: (0) 6 and 15
  - L17: (0) 12 and 15
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- Queue
- Trash

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1	☐	☑	US 5566318 A	19961015	Joseph, James D.	711/118	14	
2	☐	☑	US 5289377 A	19940222	Yokote, Timothy A. et al.	701/35	8	
3	☐	☑	US 4451880 A	19840529	Johnson, Robert B. et al.	711/157	43	

BRS form | B&R form | Hits | Details | HTML

Ready

NUM

L Number	Hits	Search Text	DB	Time stamp
7	3477946	power or voltage	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 13:05
8	457422	clock	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 13:05
9	2	(memory adj module adj controller) same (power or voltage) same clock	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 13:19
11	33	(memory adj module adj controller) same ((power or voltage) or clock)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 13:28
6	127	memory adj module adj controller	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 14:55
12	1834	module adj controller	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 14:45
13	2	("6587912").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 14:52
14	2	("6587912").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/19 14:55
15	9	("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6226762" | "6240526").PN.	USPAT	2003/08/19 14:57
16	0	(memory adj module adj controller) and (("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6226762" | "6240526").PN.)	USPAT	2003/08/19 14:56
17	0	(module adj controller) and (("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6226762" | "6240526").PN.)	USPAT	2003/08/19 14:57

EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window H

- Drafts
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  - L9: (2) 6 same 7 same 8
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  - L12: (1834) module adj controller
  - L13: (2) ("6587912").PN.
  - L14: (2) ("6587912").PN.
  - L15: (9) ("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6...
  - L16: (0) 6 and 15
  - L17: (0) 12 and 15
- Failed
- Saved
- Favorites
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- Trash

Search | List | Browse | Queue | Clear

DBs | USPAT | Plurals

Default operator: OR | Highlight all hit terms initially

("5590299" | "5854790" | "5857109" | "5860080" | "6006276" | "6073251" | "6185644" | "6226762" | "6240526").PN.

BRS form | IS&R form | Hits | Details | HTML

Ready | NUM

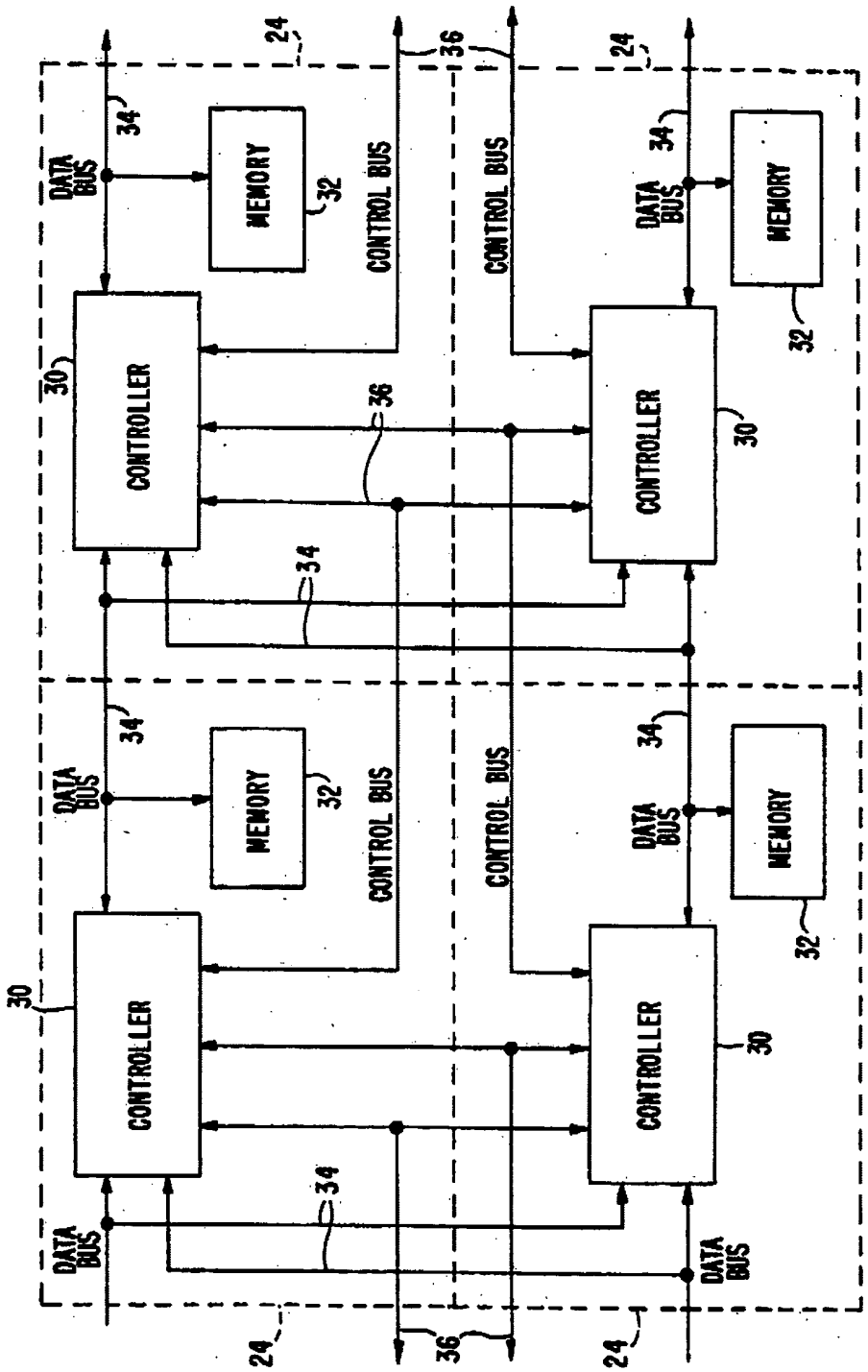


FIG. 2

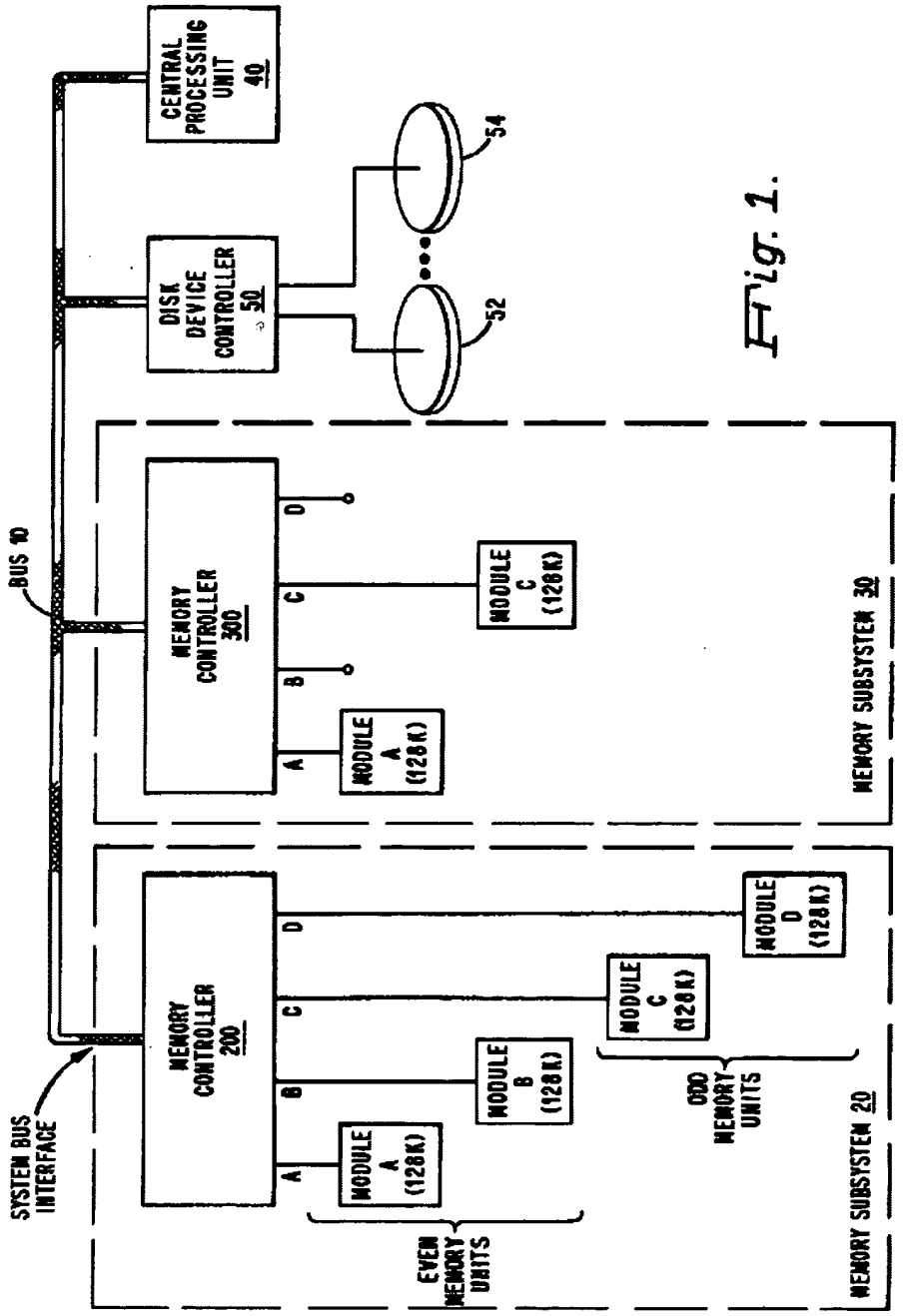


Fig. 1.

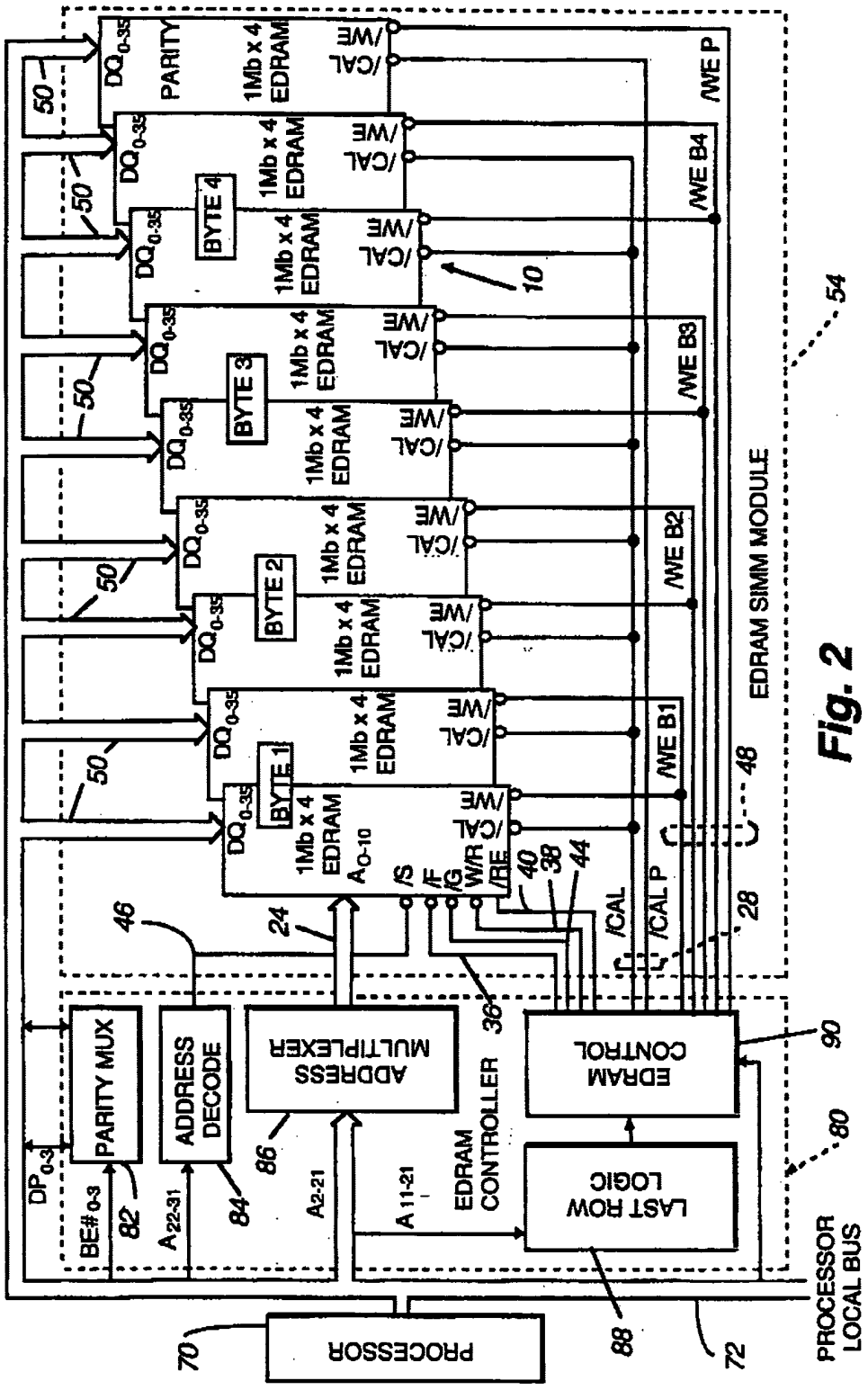


Fig. 2

US 20020145900A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2002/0145900 A1**

Schaefer (43) **Pub. Date: Oct. 10, 2002**

(54) **LOW POWER MEMORY MODULE USING RESTRICTED RAM ACTIVATION**

(76) Inventor: **Scott Schaefer**, Boise, ID (US)

Correspondence Address:
Kevin D. Martin
Micron Technology, Inc.
P.O. Box 6
Boise, ID 83707-0006 (US)

(21) Appl. No.: **10/035,728**

(22) Filed: **Dec. 20, 2001**

Related U.S. Application Data

(63) Continuation of application No. 09/652,226, filed on Aug. 29, 2000, now Pat. No. 6,359,801, which is a continuation of application No. 09/024,939, filed on Feb. 17, 1998, now Pat. No. 6,111,775, which is a continuation of application No. 08/727,836, filed on Oct. 15, 1996, now Pat. No. 5,719,817, which is a continuation of application No. 08/407,721, filed on Mar. 20, 1995, now Pat. No. 5,566,122, which is a continuation of application No. 08/000,066, filed on Jan. 4, 1993, now Pat. No. 5,414,670, which is a continuation of application No. 07/608,125, filed on Oct. 31, 1990, now Pat. No. 5,257,233.

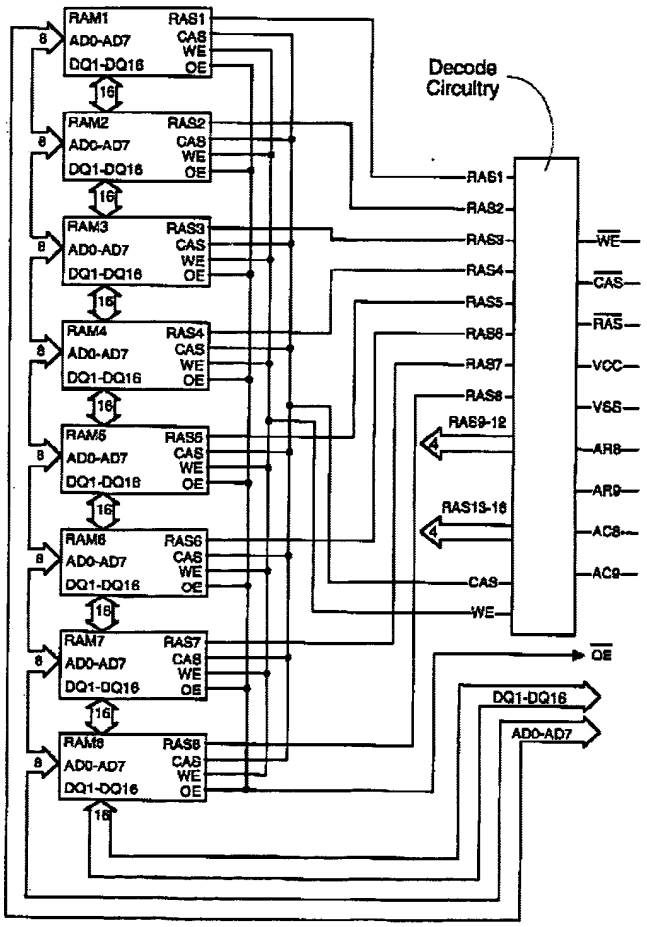
Publication Classification

(51) **Int. Cl.**[7] **G11C 5/00**

(52) **U.S. Cl.** **365/52**

(57) **ABSTRACT**

A memory module for an electronic device is disclosed which provides means for reducing the amount of power necessary to access a desired number of data bits. This provides a design of memory modules which requires fewer DRAMs to be turned on during a read or write cycle than present module designs, thereby using much less power.



DOCUMENT-IDENTIFIER: US 20020145900 A1

TITLE: Low power memory module using restricted RAM activation

-------- KWIC -------

Abstract Paragraph - ABTX (1):

A memory module for an electronic device is disclosed which provides means for reducing the amount of power necessary to access a desired number of data bits. This provides a design of memory modules which requires fewer DRAMs to be turned on during a read or write cycle than present module designs, thereby using much less power.

Summary of Invention Paragraph - BSTX (11):

[0008] An object of this invention is to provide a memory module design which uses less power than previous modules.

US006393504B1

(12) **United States Patent**
Leung et al.

(10) **Patent No.: US 6,393,504 B1**
(45) **Date of Patent: May 21, 2002**

(54) **DYNAMIC ADDRESS MAPPING AND REDUNDANCY IN A MODULAR MEMORY DEVICE**

(75) Inventors: **Wingyu Leung**, Cupertino; **Winston Lee**, South San Francisco; **Fu-Chieh Hsu**, Saratoga, all of CA (US)

(73) Assignee: **Monolithic System Technology, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/493,781**

(22) Filed: **Jan. 28, 2000**

Related U.S. Application Data

(62) Division of application No. 08/960,951, filed on Oct. 30, 1997, now Pat. No. 6,272,577, which is a division of application No. 08/549,610, filed on Oct. 27, 1995, now Pat. No. 5,729,152, which is a division of application No. 08/270,856, filed on Jul. 5, 1994, now Pat. No. 5,655,113.

(51) **Int. Cl.**[7] **G06F 13/00**; G06F 15/00; G06F 15/76

(52) **U.S. Cl.** **710/104**; 710/126; 710/129; 712/10; 712/11; 712/13; 712/14; 712/15; 712/16; 712/37

(58) **Field of Search** 710/104, 126, 710/129; 712/10, 11, 13, 14, 15, 16, 37

(56) **References Cited**

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(List continued on next page.)

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WO	WO-93/18462	9/1993
WO	WO-93/18463	9/1993

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Peter van Zant, *Microchip, A Practical Guide to Semiconductor Processing*, 1st Ed., Semiconductor Services, San Jose, CA 1986, p. 8.

MacDonald et al., "Dynamic RAMs 200mb Wafer Memory," IEEE *ISSCC*, Feb. 17, 1989, pp. 240–241 and 350.

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Stopper, "Wafer–Scale Integration," *Hybrids and High–Level Integration*, pp. 354–364.

Iscoff, "Characterizing Quickturn ASICs: It's Done with Mirrors" *Semiconductor International*, Aug. 1, 1990, pp. 68–73.

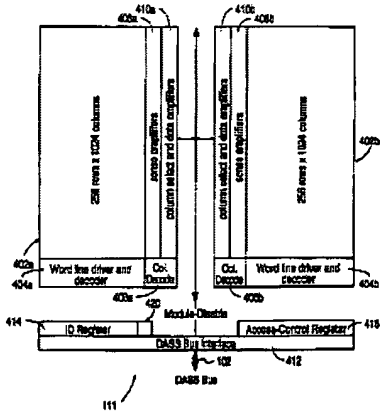
(List continued on next page.)

Primary Examiner—Ayaz Sheikh
Assistant Examiner—Frantz B. Jean
(74) *Attorney, Agent, or Firm*—Skjerven Morrill MacPherson LLP

(57) **ABSTRACT**

A memory device which utilizes a plurality of memory modules coupled in parallel to a master I/O module through a bus. Each memory module has independent address and command decoders to enable independent operation. Thus each memory module is activated by commands on the bus only when a memory access operation is performed within the particular memory module. Each memory module has a programmable identification register which stores a communication address of the module. The communication address for each module can be changed during operation of the memory device by a command from the bus. The memory device includes redundant memory modules to replace defective memory modules. Replacement can be carried out through commands on the bus.

20 Claims, 24 Drawing Sheets



L Number	Hits	Search Text	DB	Time stamp
1	16605	memory adj module	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/20 14:29
2	935937	(reduc$5 or less$5 or decreas$5 or diminish$5 or cut$5 or trim$5 or lower$5 or minimize$5 or limit$5 or curtail$5) near5 (power or voltage or frequency)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/20 14:37
3	220	(memory adj module) with ((reduc$5 or less$5 or decreas$5 or diminish$5 or cut$5 or trim$5 or lower$5 or minimize$5 or limit$5 or curtail$5) near5 (power or voltage or frequency))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/08/20 15:56

United States Patent [19]

Nielsen

[11] **Patent Number: 5,036,493**

[45] **Date of Patent: Jul. 30, 1991**

[54] **SYSTEM AND METHOD FOR REDUCING POWER USAGE BY MULTIPLE MEMORY MODULES**

[75] Inventor: **Michael J. K. Nielsen, Palo Alto, Calif.**

[73] Assignee: **Digital Equipment Corporation, Maynard, Mass.**

[21] Appl. No.: **494,672**

[22] Filed: **Mar. 15, 1990**

[51] Int. Cl.[5] **G11C 7/00**

[52] U.S. Cl. **365/230.03**; 365/230.06; 365/233

[58] Field of Search 365/230.03, 230.06, 365/230.08, 233

[56] **References Cited**

U.S. PATENT DOCUMENTS

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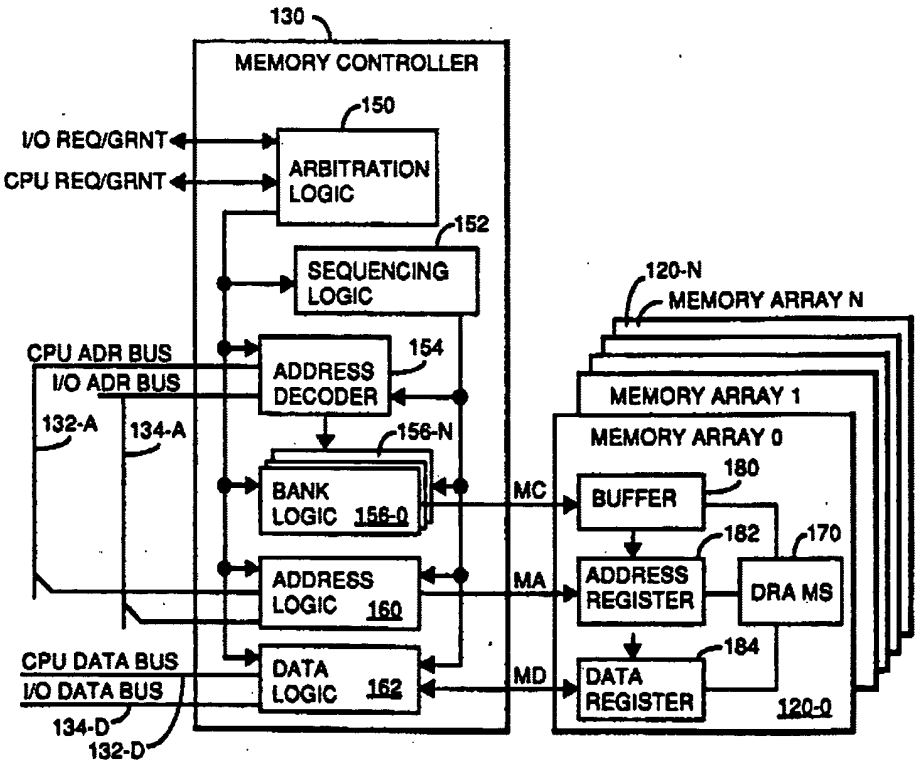
3,803,554	4/1974	Bock et al.	340/825.07
4,151,611	4/1979	Sugawara et al.	365/227
4,387,449	6/1983	Masuda	365/227
4,447,895	5/1984	Asano et al.	365/226
4,561,070	12/1985	Armstrong	365/227
4,636,982	1/1987	Takemae et al.	365/230.03
4,670,859	6/1987	Furihata et al.	365/104
4,686,651	8/1987	Armstrong et al.	365/226
4,809,234	2/1989	Kuwashiro	365/230.03
4,905,201	2/1990	Ohira et al.	365/230.03

Primary Examiner—Joseph A. Popek
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

A computer memory system has multiple memory banks, only one of which can be accessed at any one instant in time. A memory bank decoder determines which of the memory banks is being accessed. The decoded bank enable signals generated by the decoder are used to send memory clocking signals only to the memory bank which is being accessed. In addition, each memory bank includes a clocked address signal buffer and a clocked data signal buffer. Clock signals are sent only to the address and data buffers in the memory bank which is being accessed. As a result, only the selected memory bank has its address and data buffers updated. All the other memory banks remain in a quiescent state, because no control signal, address signals, or data signals are sent to those memory banks. This eliminates the energy usage that would otherwise be associated with the idle memory banks, including both the energy used by the memory chips in the idle memory banks, as well as the energy associated with changing the state of the address and data lines connected to those memory chips.

. 8 Claims, 2 Drawing Sheets



DERWENT-ACC-NO: 1988-042210

DERWENT-WEEK: 198806

TITLE: Computing low power ROM - has monostable with output connected to sync. inputs of decoder and comparator

INVENTOR: PETROVSKII, V P; SHASTIN, V A

PATENT-ASSIGNEE: KLEPIKOV I I[KLEPI]

PRIORITY-DATA: 1985SU-3863944 (February 28, 1985)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 1322376 A	July 7, 1987	N/A	003	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
SU 1322376A	N/A	1985SU-3863944	February 28, 1985

INT-CL (IPC): G11C017/00

ABSTRACTED-PUB-NO: SU 1322376A

BASIC-ABSTRACT:

The ROM is basically as described in Parent Cert., and is modified to reduce power consumption by incorporating monostable with re-start facility, the input of which is connected to the access input of the ROM and the output is connected to the sync. input of the decoder and comparator.

The monostable e.g. microcircuit type 133AGZ when using said ROM allows reduction of power demand due to disconnecting the power supply to the memory modules when there is no memory request while maintaining high speed of response.

USE - In computer engineering, partic. designing ROM's with small power demands. Bul.25/7.7.87.

CHOSEN-DRAWING: Dwg.0/1

TITLE-TERMS: COMPUTATION LOW POWER ROM MONOSTABLE OUTPUT CONNECT SYNCHRO INPUT DECODE COMPARATOR

DERWENT-CLASS: U14

EPI-CODES: U14-A06;

EAST - [kevin's workspace.wsp:1]

File View Edit Tools Window

- Drafts
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- Active
  - L1: (16605) memory adj module
  - L2: (935937) (reduc$5 or less$5 or decreas$5 or diminish$5 or cut$5 or trim$5 or lower$5 or mini...
  - L3: (220) 1 with 2
- Failed
- Saved
- Favorites
- Tagged (10)
- UDC
- Queue
- Trash

	U		Document ID	Issue Date	Inventor	Current OR	Pages
1	☐	☑	US 20020145900 A1	20021010	Schaefer, Scott	365/52	10
2	☐	☑	US 6393504 B1	20020521	Leung, Wingyu et al.	710/104	42
3	☐	☑	US 6272577 B1	20010807	Leung, Wingyu et al.	710/110	44
4	☐	☑	US 5758100 A	19980526	Odisho, Victor	710/301	6
5	☐	☑	US 5729152 A	19980317	Leung, Wingyu et al.	326/21	43
6	☐	☑	US 5655113 A	19970805	Leung, Wingyu et al.	713/401	43
7	☐	☑	US 5257233 A	19931026	Schaefer, Scott	365/227	9
8	☐	☑	US 5060188 A	19911022	Zulian, Ferruccio et al.	711/5	7
9	☐	☑	US 5036493 A	19910730	Nielsen, Michael J. K.	365/230.03	8
10	☐	☑	SU 1322376 A	19870707	PETROVSKII, V P et al.		NA

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- Tagged (7)
- UDC
- Queue
- Trash

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1	☐	☑	US 20020145900 A1	20021010	Schaefer, Scott	365/52	10
2	☐	☑	US 5758100 A	19980526	Odisho, Victor	710/301	6
3	☐	☑	US 5655113 A	19970805	Leung, Wingyu et al.	713/401	43
4	☐	☑	US 5257233 A	19931026	Schaefer, Scott	365/227	9
5	☐	☑	US 5060188 A	19911022	Zulian, Ferruccio et al.	711/5	7
6	☐	☑	US 5036493 A	19910730	Nielsen, Michael J. K.	365/230.03	8
7	☐	☑	SU 1322376 A	19870707	PETROVSKII, V P et al.		NA

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Ready NUM

INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 00/31439

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F11/00 G06F11/10 G11C5/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 744 748 A (SILICON GRAPHICS INC) 27 November 1996 (1996-11-27) page 5, line 35 -page 6, line 27; figure 3; table 1 page 12, line 40-43	1-9, 11-24
A	US 5 661 677 A (RONDEAU II THOMAS C ET AL) 26 August 1997 (1997-08-26) abstract	1-24
A	EP 0 813 204 A (SUN MICROSYSTEMS INC) 17 December 1997 (1997-12-17) abstract; figure 1A	1-24

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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(54) LOW POWER MEMORY MODULE USING RESTRICTED RAM ACTIVATION

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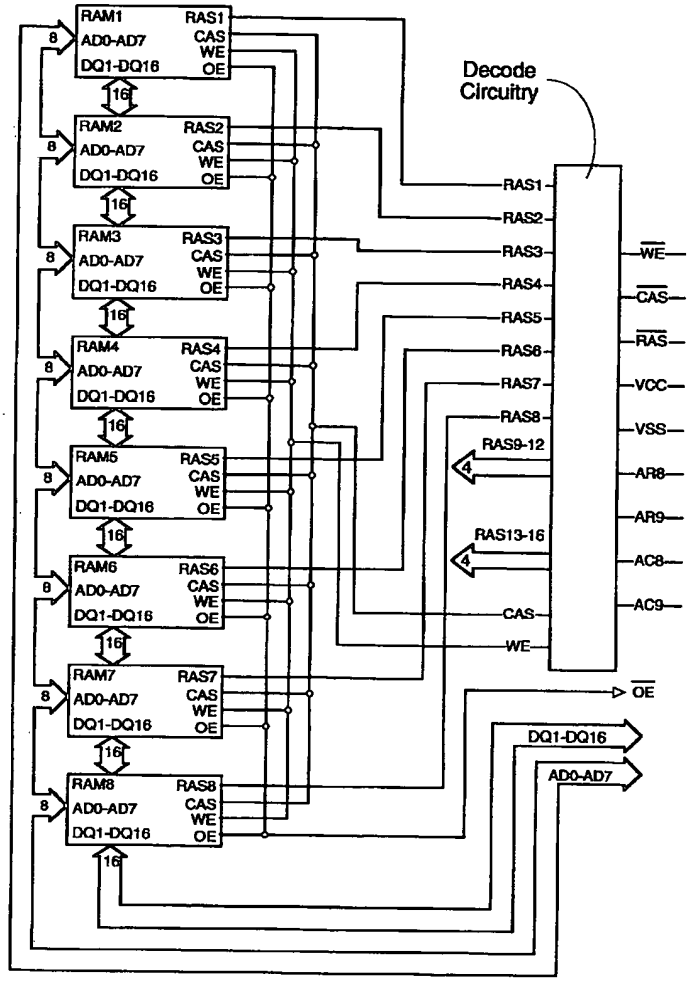
Publication Classification

(51) **Int. Cl.**[7] **G11C 5/00**

(52) **U.S. Cl.** **365/52**

(57) ABSTRACT

A memory module for an electronic device is disclosed which provides means for reducing the amount of power necessary to access a desired number of data bits. This provides a design of memory modules which requires fewer DRAMs to be turned on during a read or write cycle than present module designs, thereby using much less power.



US-PAT-NO: 5060188

DOCUMENT-IDENTIFIER: US 5060188 A

TITLE: System using registers for maintaining data address and class information from previous module accesses for predictive memory module selection

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Detailed Description Text - DETX (14):

Since at each memory operation, one and only one module is selected, the power consumption of the memory 3 is greatly reduced if compared with the prior art memories where, in order to increase the operative speed, all the memory modules are concurrently activated. Further such reduced consumption is substantially independent of the number of modules, which may be increased at will, without impact on the powering devices.

itecture in which
es are connected
patent
hained Circuit Modules"
and T. Tatematsu,
Scale Memory",
gration, January
1991, pp. 12-18. [dedicated lines]). In neither case are the circuit modules connected in parallel to a common bus.

(14) Prior art memory devices having a high I/O data bandwidth typically use several memory arrays simultaneously to handle the high bandwidth requirement. This is because the individual memory arrays in these devices have a much lower bandwidth capability than the I/O requirement. Examples of such prior art schemes include those described by K. Dosaka et al, "A 100-MHz 4-Mb Cache DRAM with Fast Copy-Back Scheme", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1534-1539; and M. Farmwald et al, PCT Patent document PCT/US91/02590.

(15) Traditional memory devices can operate either synchronously or asynchronously, but not both. Synchronous memories are usually used in systems requiring a high data rate. To meet the high data rate requirement, synchronous memory devices are usually heavily pipelined. (See, e.g., the scheme described in "250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture", Y. Takai et al, IEEE JSSC, vol. 29, no. 4, April, 1994, pp. 426-431.) The pipelined architecture disclosed in Y. Takai et al, causes the access latency to be fixed at 3 clock cycles at all clock frequencies, thereby making this synchronous memory device unsuitable for systems using lower clock frequencies. For example, when operating at 50 Mhz the device has an access latency of 60 ns (compared to an access latency of 24 ns when operating at 125 Mhz).

(16) Conventional asynchronous memory devices, due to the lack of a pipeline register, maintain a fixed access latency at all operating frequencies. However, the access cycle time can seldom be substantially smaller than the access latency. Consequently, asynchronous devices are unsuitable for high data rate applications.

(17) Thus, it would be desirable to have a memory device which provides a high through-put, low latency, high noise immunity, I/O scheme which has a symmetrical swing around one half of the supply voltage.

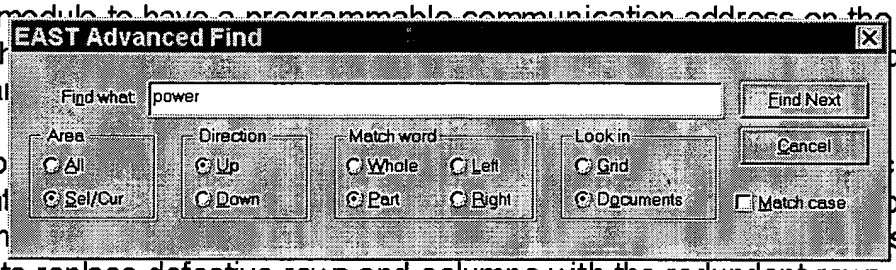
(18) It would also be desirable to have a memory device which can be-accessed both synchronously and asynchronously using the same set of connection pins.

(19) Moreover, it would be desirable to have a memory device which provides a high data bandwidth and a short access time.

(20) It would also be desirable to have a memory device which is organized into small memory arrays, wherein only one array is activated for each normal memory access, whereby the memory device has low power dissipation.

increasing the defect tolerance of the memory device. (ii) It significantly reduces power consumption of the memory device when compared to traditional memory devices because each memory access is handled completely by one memory module only with only one of the arrays activated. (iii) Since each memory module is a complete functional unit, the memory module architectures allows parallel accesses and multiple memory module operations to be performed within different memory modules, thereby increasing the performance of the memory device. (iv) The memory module architecture allows the memory device to handle multiple memory accesses at the same time.

(28) The circuit-module architecture of the present invention further allows easy system expansion by connecting multiple memory devices in parallel through a common I/O bus which is an extension of the on chip bus. In addition, by incorporating redundant memory modules on each memory device and allowing each memory module to have a programmable communication address on the I/O bus system, th[illegible]ch is better tha[illegible]



(29) In o[illegible]lude redundant[illegible]odules to support th[illegible]s also provided to replace defective rows and columns with the redundant rows and columns during operation of the memory device.

(30) The memory devices in accordance with the present invention are able to span address spaces which are not contiguous by controlling the communication addresses of the memory modules. Furthermore, the address space spanned by the memory devices can be dynamically modified both in location and size. This is made possible by the incorporation, in each memory module, of a programmable identification (ID) register which contains the base address of the memory module and a mechanism which decommissions the module from acting on certain memory access commands from the bus. The present invention therefore provides for a memory device with dynamically reconfigurable address space. Dynamically reconfigurable address space is especially useful in virtual memory systems in which a very large logical address space is provided to user programs and the logical address occupied by the programs are dynamically mapped to a much smaller physical memory space during program execution.

(31) Each memory array in the present design is equipped with its own row and column address decoders and a special address sequencer which automatically increments address of the column to be accessed. Each memory array has data amplifiers which amplify the signals read from the memory array before the signals are transmitted to the lines of the DASS bus. Both the address sequencer and data amplifiers increase the signal bandwidth of the memory array. Consequently, each memory array is capable of handling the I/O data bandwidth requirement by itself. This capability makes multiple bank operations such as broadcast-write and interleaved-access possible. For example, a memory device in accordance with the present invention is able to handle a broadcast-write bandwidth of over 36 gigabytes per second and 36 memory operations simultaneously.

(32) Memory devices in accordance with the present invention can be accessed

US-PAT-NO: 5036493

DOCUMENT-IDENTIFIER: US 5036493 A

TITLE: System and method for reducing power usage by multiple memory modules

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TITLE - TI (1):
System and method for reducing power usage by multiple memory modules

Brief Summary Text - BSTX (1):
The present invention relates generally to computer systems having two or more memory banks or modules and particularly to methods and systems for reducing the amount of power consumed by such memory modules.

US-PAT-NO: 5257233

DOCUMENT-IDENTIFIER: US 5257233 A

TITLE: Low power memory module using restricted RAM activation

--------- KWIC --------

Abstract Text - ABTX (1):

A memory module for an electronic device is disclosed which provides means for reducing the amount of power necessary to access a desired number of data bits. This provides a design of memory modules which requires fewer DRAMs to be turned on during a read or write cycle than present module designs, thereby using much less power.

Brief Summary Text - BSTX (11):

An object of this invention is to provide a memory module design which uses less power than previous modules

US-PAT-NO: 5758100

DOCUMENT-IDENTIFIER: US 5758100 A

TITLE: Dual voltage module interconnect

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Brief Summary Text - BSTX (4):

Computer systems and computer components are being developed to operate using lower and lower voltages. It is currently typical for older systems to operate with 5 volts and for newer systems to operate with 3.3 volts. As systems are developed to operate with lower voltages, problems of compatibility between systems and add-on components can occur. For example, a purchaser of a new system using a lower voltage than the old one may wish to continue using add-on memory modules from the old system because buying new memory modules would be expensive. Even though 3.3 volt systems are able to supply both 3.3 and 5 volts to components, current 3.3 volt systems incur difficulties when using previous, 5 volt components. For example, it may be necessary to provide special component sockets and cards for each voltage to prevent a component card from inadvertently being inserted in a socket with an improper voltage, causing it to be damaged. Supplying extra sockets on a system printed circuit board, however, uses up board space, which should be avoided.